CLAIMS

While the invention has been described with reference to particular example embodiments, further modifications and improvements which will occur to those skilled in the art, may be made within the purview of the appended claims, without departing from the scope of the invention in its broader aspect.
Numerous modification and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

What is claimed is:

1. A synchronous sequential processor (SSP) for processing of a wave-form, wherein:
said processed wave-form is captured using a sampling clock;
said wave-form is processed by multiple sequential processing stages, wherein an output of any earlier stage is connected to an input of a later stage.
2. An SSP as claimed in claim 1 wherein:
said sequential processing stages are driven by clocks which are synchronous to the sampling clock or to clocks derived by dividing a frequency of the sampling clock by an integer.
3. An SSP as claimed in claim 2, wherein said synchronous clocks are derived by dividing a frequency of said sampling clock and/or its sub-clocks generated by the outputs of serially connected gates which the sampling clock is propagated through.
4. An SSP as claimed in claim 1, wherein:
the wave-form is captured using a delay line built with serially connected gates or with other serially connected delay elements.
5. An SSP as claimed in claim 1, wherein said wave-form capturing comprises:
capturing of incoming wave-form level with a sampling clock and its sub-clocks generated by the outputs of serially connected gates which the sampling clock is propagated through;
or capturing the outputs of serially connected gates which the incoming wave-form is propagated through, with the sampling clock;
or capturing the sampling clock with the outputs of serially connected gates which the incoming wave-form is propagated through;
or capturing the outputs of serially connected gates which the sampling clock is propagated through, with the incoming wave-form.
6. An SSP as claimed in claim 4, wherein said serially connected gates:
are connected as an open ended delay line;
or are connected into a ring oscillator which can be controlled in a PLL configuration;
or are connected into a delay line which can be controlled in a delay locked

loop (DLL) configuration.

7. An SSP as claimed in claim 1, wherein the SSP comprises multiphase wave-form captures which allow wave-form levels which correspond to consecutive cycles of a sampling clock to be captured in different consecutive registers for further processing.

8. An SSP as claimed in claim 1, using said sampling clock and its sub-clocks, generated by the outputs of serially connected gates which the sampling clock is propagated through, for implementing said multiphase wave-form captures.

9. An SSP as claimed in claim 8, using serially connected clock selectors for enabling sub-clocks performing wave-form captures during particular phases, wherein:
falling edges of said sub-clocks are used for driving clock selectors which select parallel processing phases during which positive sub-clocks are enabled to perform waveform capturing;
or rising edges of said sub-clocks are used for driving selectors which select parallel processing phases during which negative sub-clocks are enabled to perform waveform capturing.

10. An SSP as claimed in claim 4, comprising measuring time intervals between active wave form edges; wherein:
an active edge of the wave-form is detected by capturing a change in a wave-form level by one of the sub-clocks;
said edge capturing sub-clock defines an edge skew between an edge of the sampling clock and the wave-form edge;
said time intervals are measured as being composed of said edge skew of a front edge of the incoming waveform, an integer number of sampling clock periods between the front edge and an end edge, and said edge skew of the end edge of the wave-form.

11. An SSP as claimed in claim 1, comprising multiple parallel processing phases; wherein:
parallel processing phases are driven by clocks having two or more times lower frequencies than said sampling clock;
consecutive parallel phases are driven by clocks which are shifted in time by one or more periods of said sampling clocks.

12. An SSP as claimed in claim 11, using said sampling clock and its sub-clocks, generated by the outputs of serially connected gates which the sampling clock is propagated through, for driving said multiple parallel processing phases.

13. An SSP as claimed in claim 12, using serially connected clock selectors for enabling sub-clocks which drive individual parallel processing phases, wherein:
falling edges of said sub-clocks are used for driving clock selectors which select parallel processing phases during which positive sub-clocks are enabled;
or rising edges of said sub-clocks are used for driving selectors which select parallel processing phases during which negative sub-clocks are enabled.

14. An SSP as claimed in claim 11, comprising merging of said parallel processing phases; wherein:
said multiple parallel processing phases are merged into a smaller number of

parallel phases or into a single processing phase, when passing from a one sequential processing stage to a next sequential stage.

15. An SSP as claimed in claim 11, comprising splitting of said parallel processing phases; wherein:
a one processing phase is split into multiple parallel processing phases or multiple parallel processing phases are split into even more parallel phases, when passing from a one sequential processing stage to a next sequential stage.

16. An SSP as claimed in claim 13, comprising time sharing of said parallel processing phases; wherein:
a task of processing of a newly captured wave-form edge or a newly began wave-form pulse, is assigned to a next available parallel processing phase.

17. An SSP as claimed in claim 16, wherein:
active edges of said captured wave-form are decoded;
said sub-clocks enabled to drive parallel processing phases and said decoding of the active edges, are used for performing said time sharing phase assignments and for further control of operations of already assigned phase.

18. An SSP as claimed in claim 13, the SSP comprising:
passing outputs of a one parallel processing phase to a next parallel phase;
using said passed outputs for processing conducted by a following sequential processing stage which belongs to the next parallel processing phase.

19. An SSP as claimed in claim 18, the SSP further comprising:
re-timing output register bits of the original parallel phase, by clocking them into an output register of the next parallel phase simultaneously with processing results of the next parallel phase.

20. An SSP as claimed in claim 1, comprising multiple parallel processing stages; wherein:
multiple parallel processing stages, performing different logical or arithmetical operations, are driven by the same clock which is applied simultaneously to all the parallel stages.

21. An SSP as claimed in claim 20, comprising merging of said parallel processing stages; wherein:
said multiple parallel processing stages are merged into a smaller number of parallel stages or into a single processing stage, when passing from one sequential processing stage to the next sequential stage.

22. An SSP as claimed in claim 20, comprising splitting of said parallel processing stages; wherein:
a one processing stage is split into multiple parallel processing stages or multiple parallel processing stages are split into even more parallel stages, when passing from a one sequential processing stage to a next sequential stage.

23. An SSP as claimed in claim 1, wherein:
said sequential processing stages use selectors and/or arithmometers and/or output registers.

24. An SSP as claimed in claim 23, wherein:

said selectors select constant values or outputs of previous sequential stages or outputs of preceding parallel stages or an output of the same stage.

25. An SSP as claimed in claim 24, wherein:
outputs of said selectors provide inputs for said arithmometer;
said arithmometer output is clocked-in to an output register by a clock which is synchronous to the sampling clock or to the sampling clock divided by an integer.

26. An SSP as claimed in claim 23, wherein:
inputs of multiple arithmometers are provided with constant values or outputs of previous stages or outputs of parallel stages or an output of the same stage.

27. An SSP as claimed in claim 26, wherein:
outputs of said arithmometers provide inputs for said selector;
said selector output is clocked-in to an output register by a clock which is synchronous to the sampling clock or to the sampling clock divided by an integer.

28. An SSP as claimed in claim 20, wherein:
said sequential processing stages use selectors and/or arithmometers and/or output registers;
outputs of said selectors which belong to one parallel processing stage, are used for controlling functions of other selectors which belong to other parallel processing stage.

29. A digital signal processing of multi-sampled phase (DSP MSP), wherein:
multiple samples of a signal are captured per a symbol time;
said samples are captured using a sampling clock and its sub-clocks, which provide known phase displacements versus the sampling clock;
said samples are captured and processed by multistage circuits.

30. A DSP MSP as claimed in claim 29, wherein;
said multistage circuits are driven by said sampling clock and said sub-clocks;
said multistage circuits are decoding active edges of the signal and results of the decoding are used for controlling operations of the multistage circuits.

31. A DSP MSP as claimed in claim 29, wherein:
a clock synthesizer circuit which may comprise a PLL or a DLL, is used for producing said sampling clock which maintains frequency or phase alignment with the clock which drives the incoming wave-form.

32. A DSP MSP as claimed in claim 29, wherein:
current phase skews between the sampling clock and the wave-form driving clock are derived from captured wave-form samples;
said current phase skews, are used to correct processing of captured signals and/or decoding of incoming signal data patterns.

33. A DSP MSP as claimed in claim 29, wherein:
said multistage signal processing comprises a sequence of basic stages performing specific arithmetic operations;
output of a previous basic stage is provided as input of a current basic stage which provides an input for the next basic stage as well.

34. A fractional bit staffing (FBS),wherein:
a series of input arguments is provided for a repeatedly performed arithmetic operation;
a series of multiple binary terms is used for supplementing said input arguments with binary values defined by corresponding terms.

35. An FBS as claimed in claim 34, wherein:
said series of multiple binary terms is downloaded to a register;
a circuit which performs said arithmetic operation uses said terms, by shifting the register during any operation and accessing the same portion of the register.

36. An FBS as claimed in claim 34, wherein:
said series of multiple binary terms is downloaded to a register;
a circuit which performs said arithmetic operation uses said terms, by using a selector circuit which selects a consecutive portion of the register which contains the corresponding terms.

37. An FBS as claimed in claim 34, wherein:
Said FBS is used for extending a precision of arithmetic operations.

38. An FBS as claimed in claim 34, wherein:
Said FBS is used for correcting predictable errors introduced by an input signal capturing and/or a signal processing.

39. A DSP MSP as claimed in claim 29, wherein the DSP MSP comprises:
detection of captured edges of a signal;
calculating whole time intervals between said captured edges, which define duration of pulses of a signal wave-form;
using said whole time intervals, for further signal processing and/or data recovery.

40. A DSP MSP as claimed in claim 29, wherein the DSP MSP comprises:
detection of captured edges of a signal;
encoding phase differences between said captured edges and edges which are expected based on an estimate of a symbol time and/or based on a prediction of a signal wave-form for a particular type of signal;
using said phase differences for further signal processing and/or data recovery.

41. A DSP MSP as claimed in claim 29, the DSP MSP comprising noise filters for digital filtering of a captured wave-form.

42. A DSP MSP as claimed in claim 41, wherein the DSP MSP comprises:
a filter mask register which provides a pattern which can be compared with a content of a register which contains a captured wave-form of an input signal;
a filter arithmometer which uses the mask registers content for corrections of captured wave-forms.

43. A DSP MSP as claimed in claim 42, wherein the DSP MSP comprises:
filter control register which provides code which controls said filter arithmometer operations for said corrections of captured wave-forms.

44. A DSP MSP as claimed in claim 29, the DSP MSP comprising multiple parallel processing phases and multiple sequential processing stages; wherein:

parallel processing phases are driven by clocks having two or more times lower frequencies than said sampling clock;
consecutive parallel phases are driven by clocks which are shifted in time by one or more periods of said sampling clocks;
said captured signal samples are processed by multiple sequential processing stages, wherein an output of any earlier stage is connected to an input of a later stage.

45. A DSP MSP as claimed in claim 42 and in claim 44, the DSP MSP comprising a second noise filtering sequential stage in every noise filtering parallel phase for extending a range of a filtered wave-form beyond a boundary of a single phase.

46. A DSP MSP as claimed in claim 45, wherein the second noise filtering sequential stage comprises:
a filter mask register which provides a pattern which can be compared with a content of a register which contains a captured wave-form of an input signal;
a filter arithmometer which uses the mask register content for corrections of captured wave-forms.

47. A DSP MSP as claimed in claim 46, wherein:
carry over bit or bits of an output register of said first filter stage of one phase is clocked-in into an output register of the first filter stage of a next phase together with filtering results of the next phase;
the second filter stage of the next phase uses the output register of the first stage for filtering a wave-form interval which extends through both said phases.

48. A DSP MSP as claimed in claim 46, wherein the second noise filtering sequential stage comprises:
filter control register which provides code which controls said filter arithmometer operations for said corrections of captured wave-forms.

49. A DSP MSP as claimed in claim 29, the DSP MSP comprising phase processing stages (PPS) of the captured wave-form; wherein:
an active edge of the wave-form is detected by capturing a change in a wave-form level by one of the sub-clocks;
said edge capturing sub-clock defines an edge skew between an edge of the sampling clock and the wave-form edge;
pulse duration is measured as being composed of said edge skew of a front edge of the incoming waveform, an integer number of sampling clock periods between the front edge and an end edge, and said edge skew of the end edge of the wave-form.

50. A DSP MSP as claimed in claim 49, the DSP MSP further comprising:
calculating the front edge skew and the end edge skew of the in-coming wave-form pulses;
combining said edge skews with other indicators of pulse duration and phase deviations between the sampling clock and a clock which generates the incoming wave-form;
evaluating the resulting timing of the incoming wave-form pulses versus

expected timing values which correspond to interpretation patterns of the incoming signal;
using results of the above mentioned operations for controlling said multistage circuits for processing of an input signal.

51. A DSP MSP as claimed in claim 29, the DSP MSP comprising periodical skew accumulation circuits (PSA); wherein:
a periodical skew estimates a phase skew between the sampling clock period versus an expected period of a clock which drives the incoming signal;
the PSA calculates accumulations of said periodical skews for single pulses or for combinations of pulses of the incoming signal;

52. A DSP MSP as claimed in claim 51, wherein;
said PSA reads a next set of said periodical skews from other circuits, and attaches them to a present set of the periodical phase skews;
said accumulations of the pulse skews are used by other input signal processing circuits.

53. A DSP MSP as claimed in claim 29, comprising received data collection (RDC) for recovering and registering data which is provided in said captured signal.

54. A DSP MSP as claimed in claim 53, wherein:
the recovered data is collected in a data buffer comprising fixed number of bits or bytes, before being transferred to other circuits.

55. A DSP MSP as claimed in claim 29, comprising a data frequency capturing (DFC) for recovering and capturing a frequency of a clock of said captured signal.

56. A DSP MSP as claimed in claim 55, further comprising:
measuring time intervals of incoming signal pulses;
defining, measured in sampling clocks, expected time intervals for data patterns provided by the incoming signal pulses;
using said measured and defined intervals, for a frequency estimation of the captured signal clock;
or using a difference between said measured and defined intervals, for a frequency estimation of the captured signal clock.

57. A DSP MSP as claimed in claim 29, comprising a wave-form screening and capturing circuits (WFSC), for verification of said captured wave-form for compliance or non-compliance with programmable patterns.

58. A DSP MSP as claimed in claim 57, the DSP MSP comprising:
using programmable screening masks and/or programmable control codes for verifying incoming wave-form captures for compliance or non-compliance with said programmable screening patterns.

59. A DSP MSP as claimed in claim 58, further comprising:
buffering captured wave-form for which the pre-programmed compliance or non-compliance have been detected;

and/or counting a number of said detections;
communicating said buffered wave-form and/or a detections counter, to an internal control circuit and/or to an external unit.

60. A DSP MSP as claimed in claim 59, comprising :
using programmable time slot selection circuits for selecting a time interval for which incoming wave-form captures shall be buffered and communicated to an internal control circuit and/or to an external unit.

61. A DSP MSP as claimed in claim 29, comprising a programmable control unit (PCU) for reading results of captured signal processing from said multistage circuit and for controlling operations of the multistage circuit.

62. A DSP MSP as claimed in claim 61, wherein the PCU comprises using adaptive signal processing algorithms for controlling operations of the multistage circuit.

63. A DSP MSP as claimed in claim 61, wherein the PCU comprises programming of noise filtering masks and/or noise filtering functions, which are applied for filtering of captured wave-forms.

64. A DSP MSP as claimed in claim 61, wherein the PCU comprises:
programming of verification patterns for checking captured wave-forms for compliance or non-compliance with the patterns;
and/or programming of verification functions which control operations which implement said checking of captured wave-forms;
and/or reading verification results and reading captured wave-forms which correspond to the preprogrammed verification criteria;
and/or reading captured wave-forms which can be pre-selected by the PCU arbitrarily and/or based on other inputs from the multistage circuit.

65. A DSP MSP as claimed in claim 29, comprising sequential data recovery from multi-sampled phase (SDR MSP) for recovering data from said captured signal.

66. A DSP MSP as claimed in claim 65, wherein the SDR MSP comprises:
detection of phases of rising and falling edges of the received signal;
using said phases of signal edges for evaluating lengths of a pulse of the received signal;
using said evaluation of the pulse lengths for calculating a number of data bits received in the pulse.

67. A DSP MSP as claimed in claim 65, wherein the SDR MSP comprises:
digital filters for filtering out noise from said captured signal.